US009437572B2

(12) United States Patent
Chen et al.

(10) Patent No.: US 9,437,572 B2
(45) Date of Patent: Sep. 6, 2016

(54) **CONDUCTIVE PAD STRUCTURE FOR HYBRID BONDING AND METHODS OF FORMING SAME**

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( * ) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 155 days.

(21) Appl. No.: **14/133,328**

(22) Filed: **Dec. 18, 2013**

(65) **Prior Publication Data**

US 2015/0171050 A1 Jun. 18, 2015

(51) **Int. Cl.**

| | |
|---|---|
| ***H01L 23/48*** | (2006.01) |
| ***H01L 23/52*** | (2006.01) |
| ***H01L 23/00*** | (2006.01) |
| ***H01L 21/324*** | (2006.01) |
| ***H01L 27/146*** | (2006.01) |
| ***H01L 21/311*** | (2006.01) |
| ***H01L 21/321*** | (2006.01) |

(52) **U.S. Cl.**

CPC ......... ***H01L 24/80*** (2013.01); ***H01L 21/31144*** (2013.01); ***H01L 21/324*** (2013.01); ***H01L 21/3212*** (2013.01); ***H01L 24/02*** (2013.01); ***H01L 24/03*** (2013.01); ***H01L 24/05*** (2013.01); ***H01L 24/08*** (2013.01); ***H01L 27/1464*** (2013.01); ***H01L 27/1469*** (2013.01); ***H01L 27/14634*** (2013.01); *H01L 2224/0235* (2013.01); *H01L 2224/02321* (2013.01); *H01L 2224/039* (2013.01); *H01L 2224/0345* (2013.01); *H01L 2224/03452* (2013.01); *H01L 2224/03462* (2013.01); *H01L 2224/03614* (2013.01); *H01L 2224/03845* (2013.01); *H01L 2224/05553* (2013.01); *H01L 2224/05554* (2013.01); *H01L 2224/05555* (2013.01); *H01L 2224/05556* (2013.01); *H01L 2224/05557* (2013.01); *H01L 2224/05559* (2013.01); *H01L 2224/05569* (2013.01); *H01L 2224/05576* (2013.01); *H01L 2224/05647* (2013.01);

(Continued)

(58) **Field of Classification Search**

CPC .............................................. H01L 2221/1063
USPC ......................................................... 257/784
See application file for complete search history.

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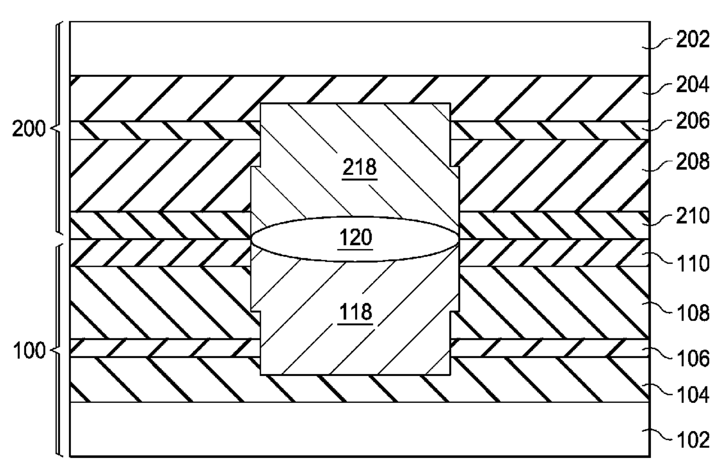
(57) **ABSTRACT**

A method embodiment includes patterning an opening through a layer at a surface of a device die. The method further includes forming a liner on sidewalls of the opening, patterning the device die to extend the opening further into the device die. After patterning the device die, the liner is removed. A conductive pad is formed in the device die by filling the opening with a conductive material.

**20 Claims, 7 Drawing Sheets**



(52) **U.S. Cl.**
CPC ............... *H01L 2224/05687* (2013.01); *H01L 2224/08057* (2013.01); *H01L 2224/08145* (2013.01); *H01L 2224/80011* (2013.01); *H01L 2224/80013* (2013.01); *H01L 2224/80121* (2013.01); *H01L 2224/80895* (2013.01); *H01L 2224/80896* (2013.01); *H01L 2224/80906* (2013.01); *H01L 2224/80948* (2013.01)

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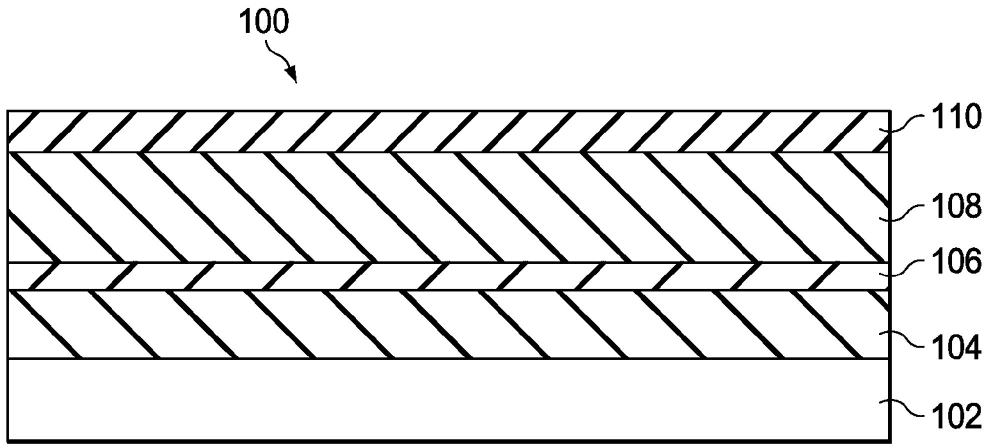


FIG. 1

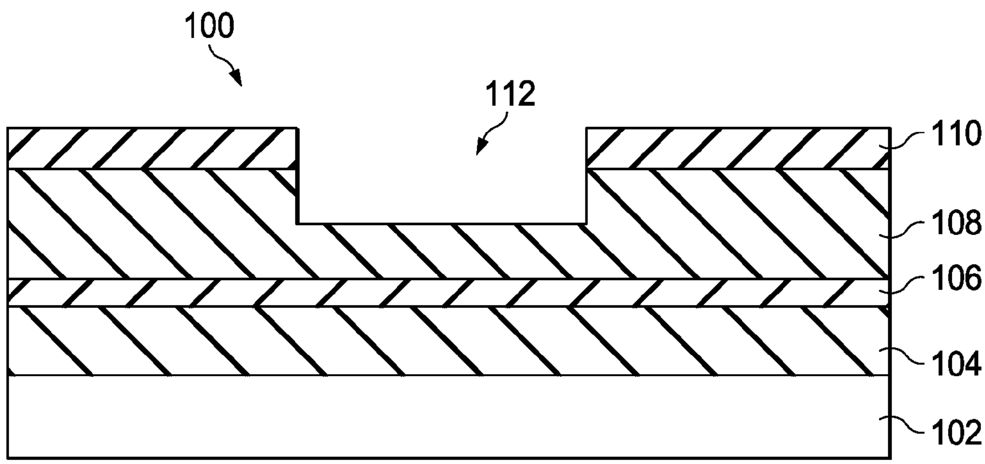


FIG. 2

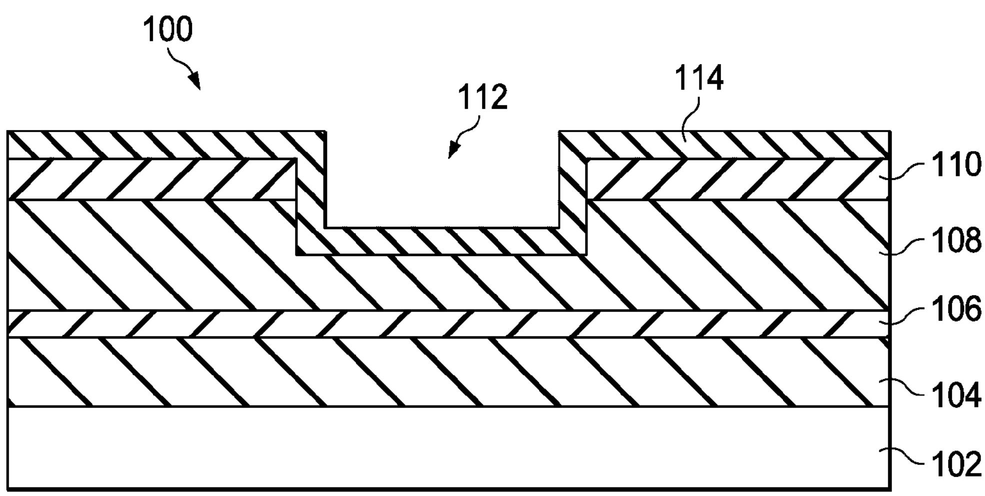


FIG. 3

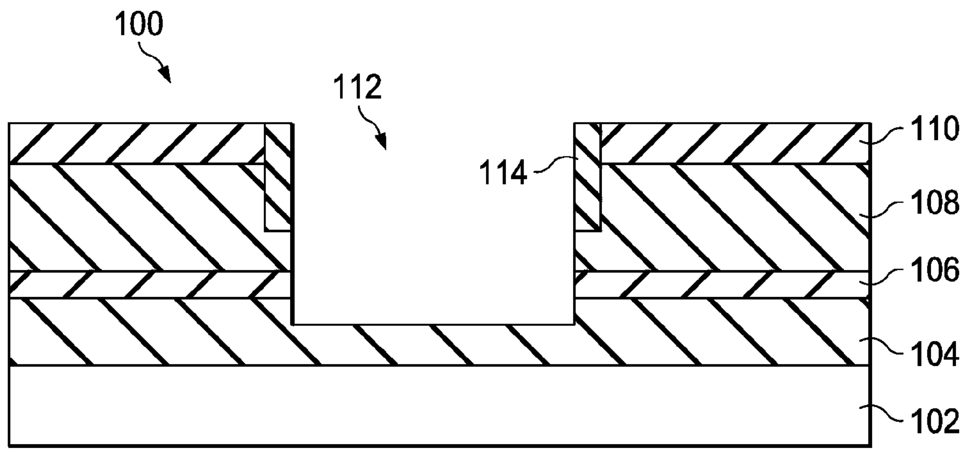


FIG. 4

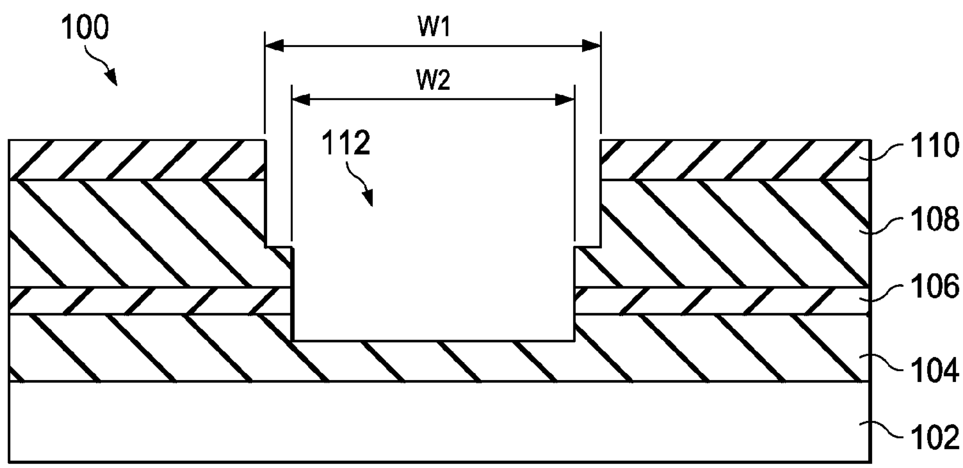


FIG. 5

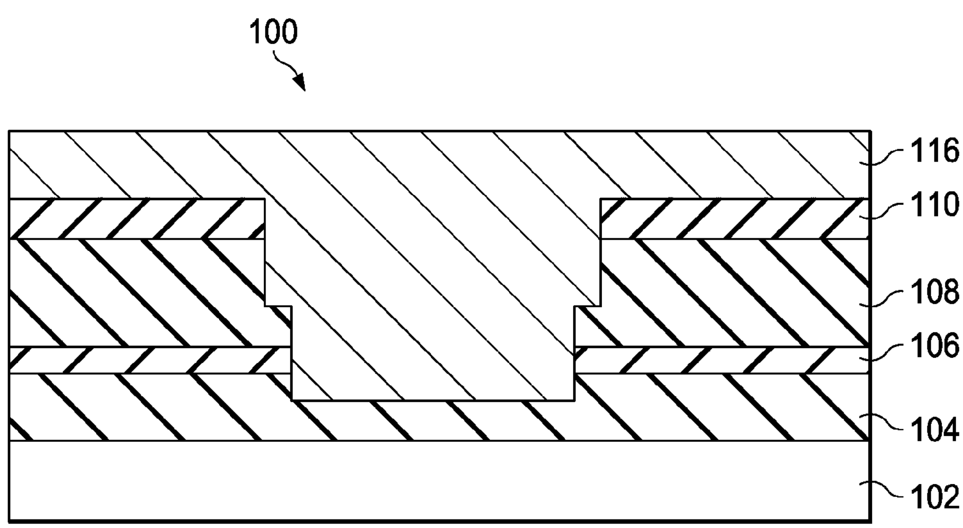


FIG. 6

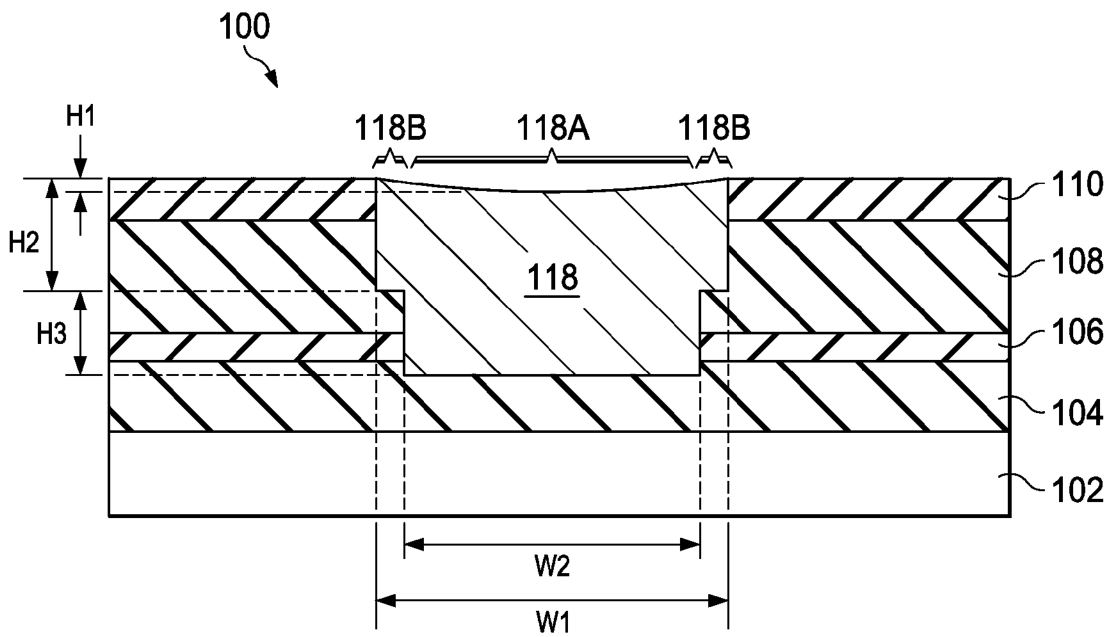
100
H1
H2
H3
118B
118A
118B
118
110
108
106
104
102
W2
W1

FIG. 7

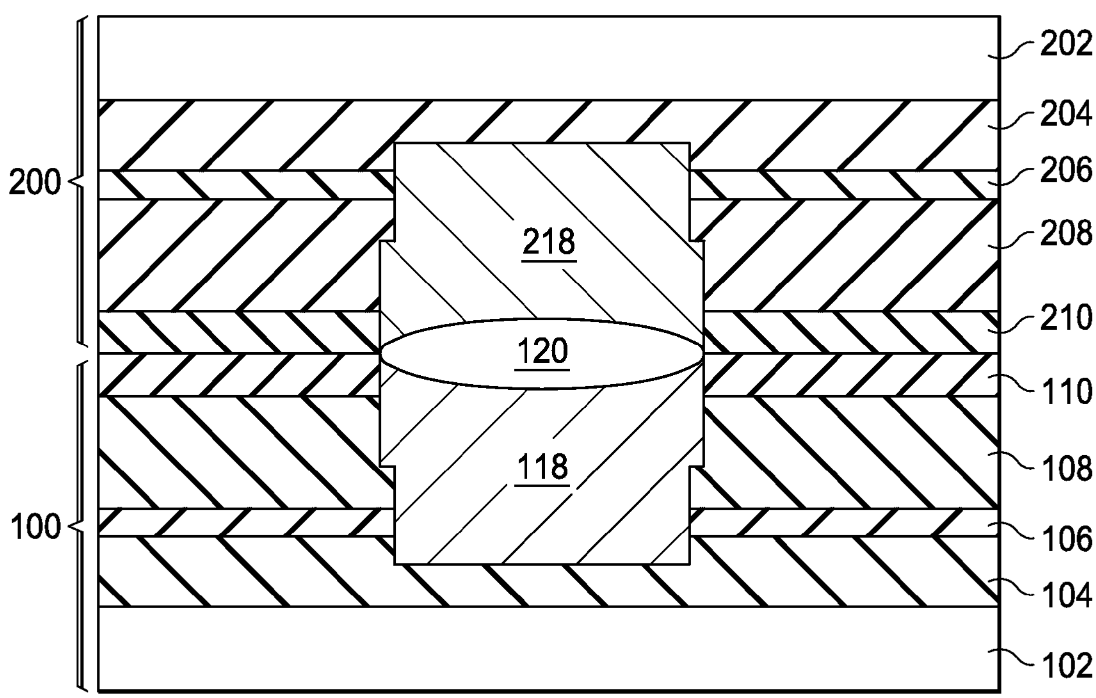
200
100
218
120
118
202
204
206
208
210
110
108
106
104
102

FIG. 8A

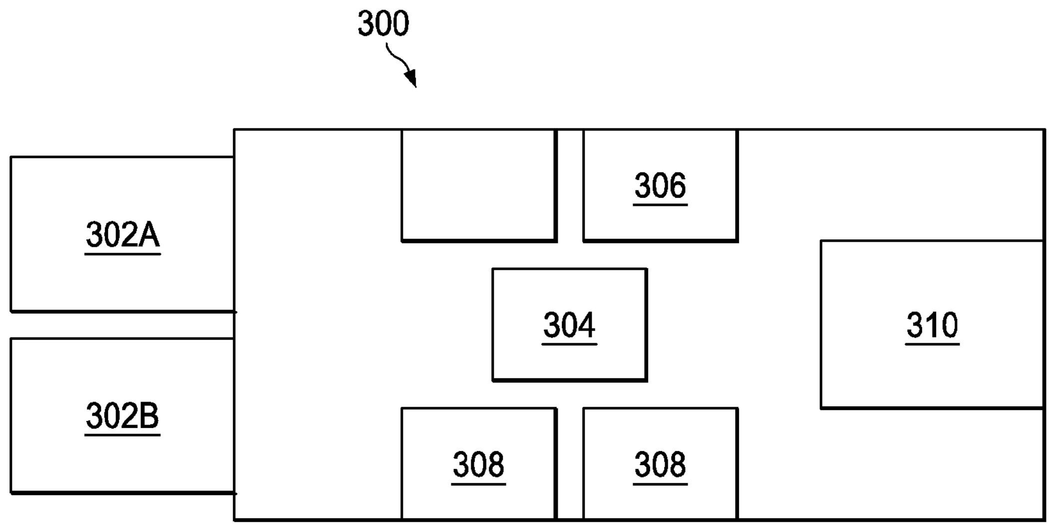
300
302A
302B
306
304
310
308
308

FIG. 8B

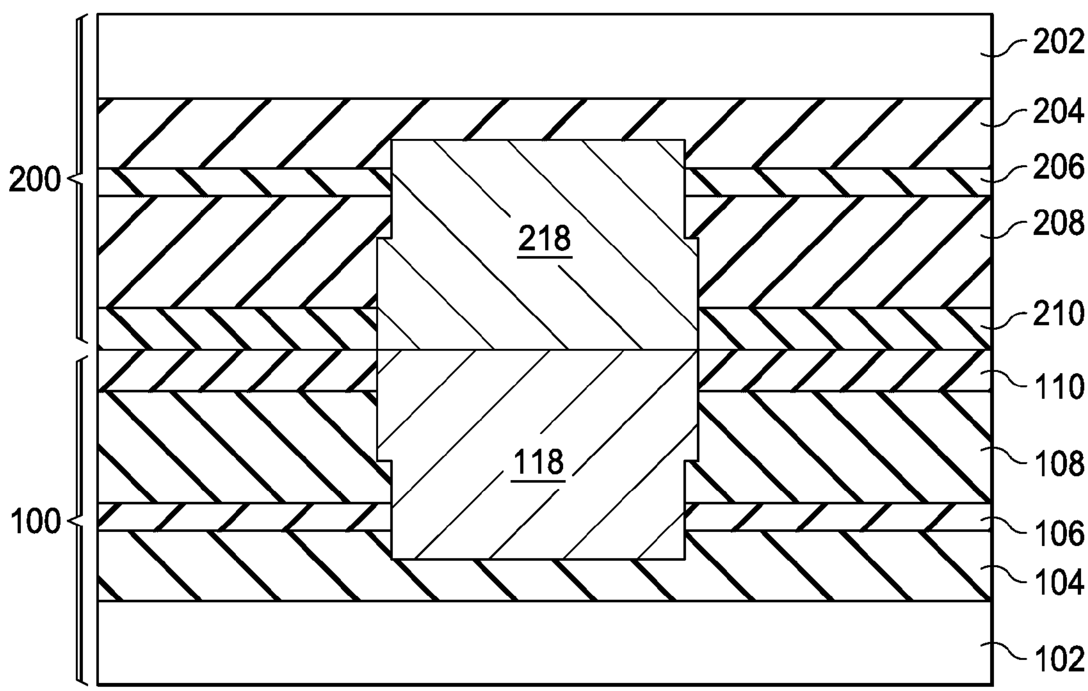
200
100
218
118
202
204
206
208
210
110
108
106
104
102

FIG. 9

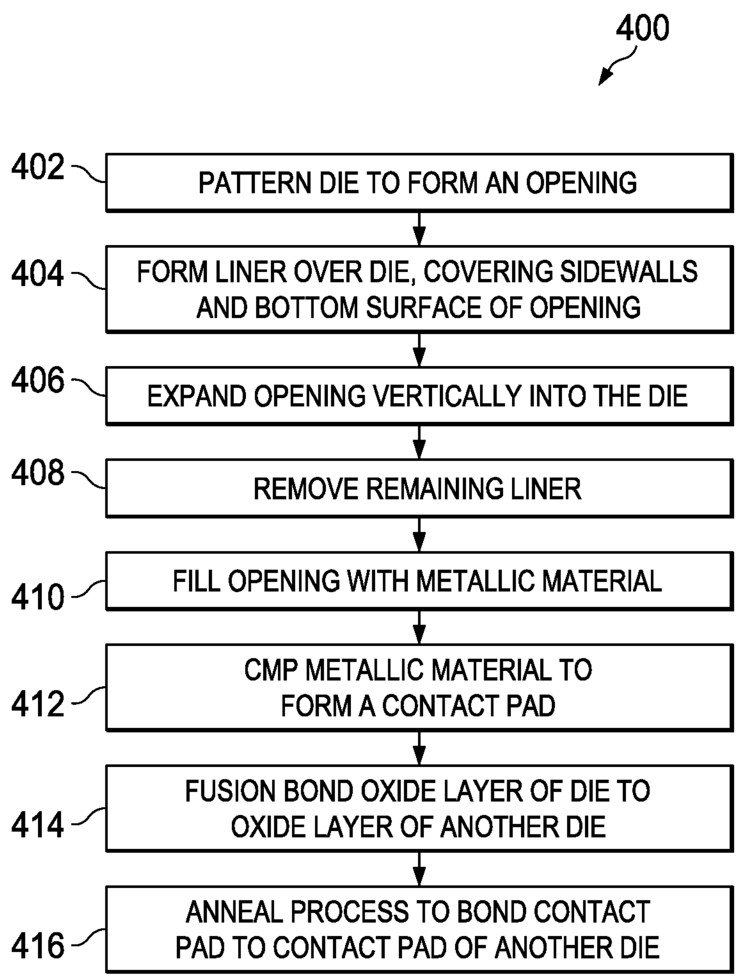
400
402
PATTERN DIE TO FORM AN OPENING
404
FORM LINER OVER DIE, COVERING SIDEWALLS AND BOTTOM SURFACE OF OPENING
406
EXPAND OPENING VERTICALLY INTO THE DIE
408
REMOVE REMAINING LINER
410
FILL OPENING WITH METALLIC MATERIAL
412
CMP METALLIC MATERIAL TO FORM A CONTACT PAD
414
FUSION BOND OXIDE LAYER OF DIE TO OXIDE LAYER OF ANOTHER DIE
416
ANNEAL PROCESS TO BOND CONTACT PAD TO CONTACT PAD OF ANOTHER DIE

FIG. 10

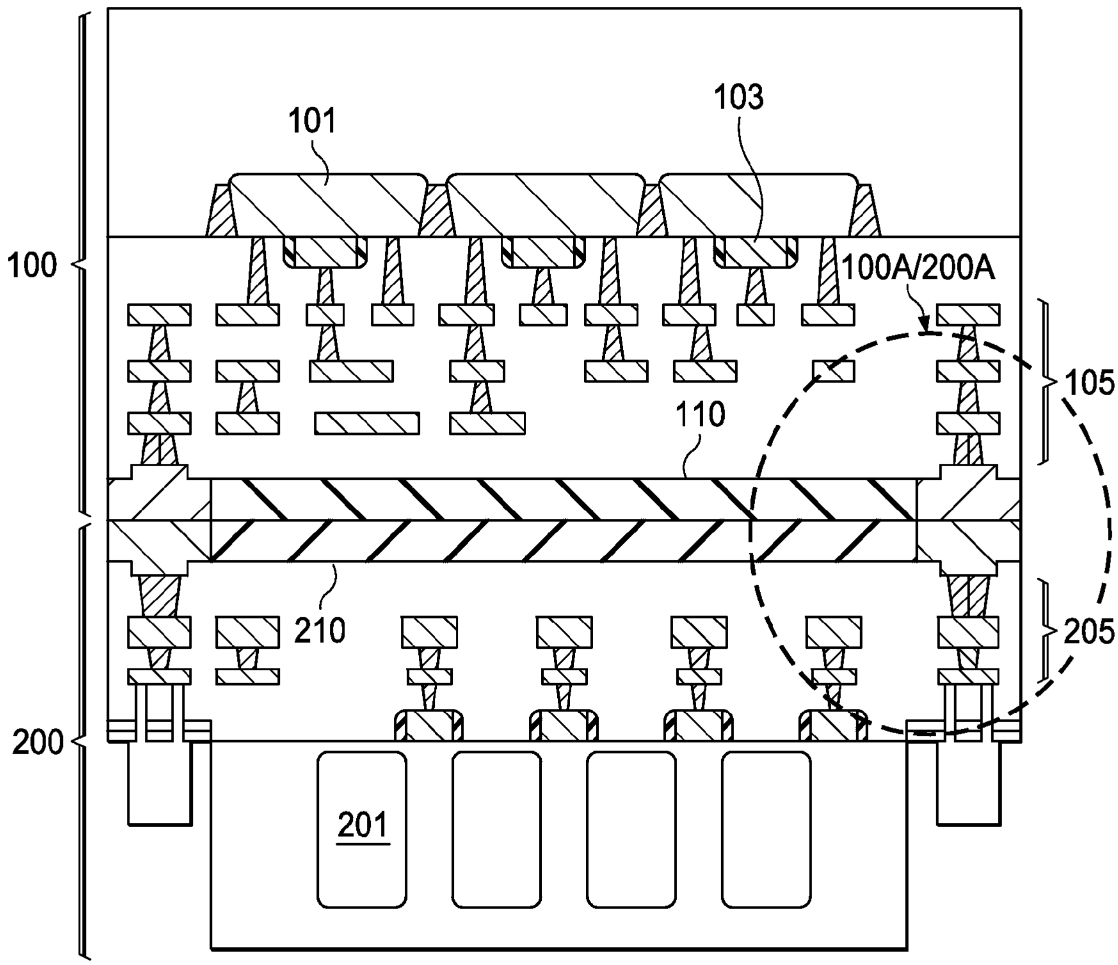


FIG. 11A

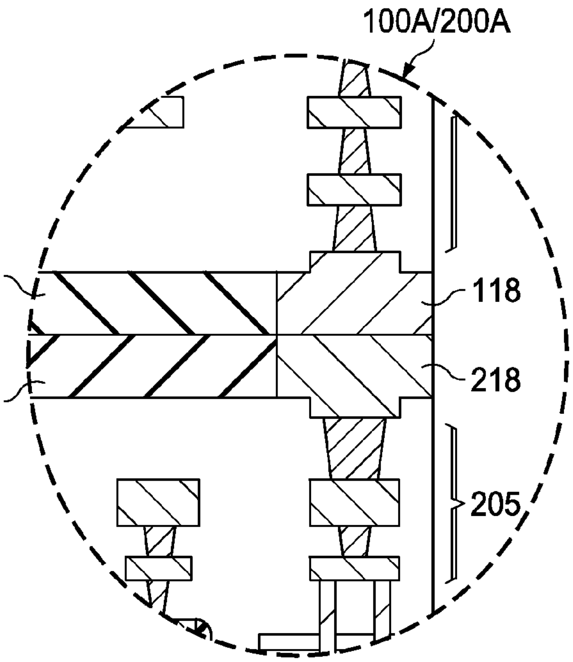


FIG. 11B

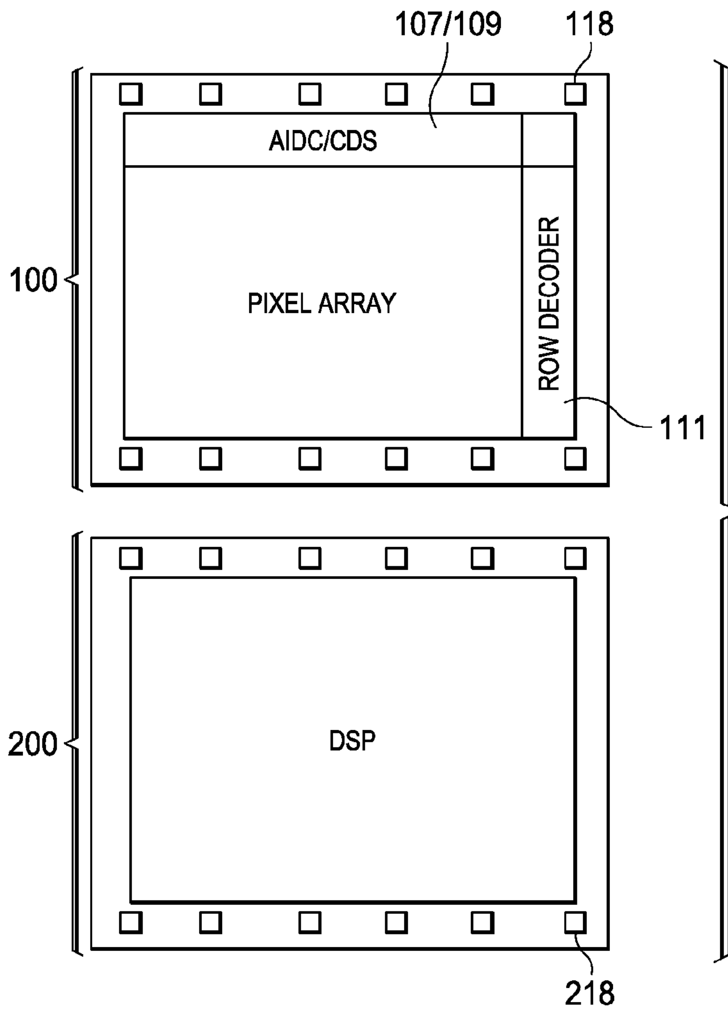


FIG. 11C

# CONDUCTIVE PAD STRUCTURE FOR HYBRID BONDING AND METHODS OF FORMING SAME

## TECHNICAL FIELD

The present invention relates generally to bonding, and, in particular embodiments, a conductive pad structure for hybrid bonding and methods of forming same.

## BACKGROUND

Typically, in a semiconductor device, various electronic components (e.g., transistors, diodes, resistors, capacitors, and the like) are formed in device dies on a wafer. These device dies may then be sawed and bonded to other device dies to form functional devices. For example, in image sensing technologies, a complementary metal-oxide semiconductor (CMOS) image sensor (CIS) may include pixel arrays (e.g., connected to photo diodes) formed on one device die, and logical control circuits may be formed on another device die. These separate dies may be bonded together using a hybrid bonding process to form a functional device. Hybrid bonding is also used in other applications to form three dimensional integrated circuits (3DICs) where multiple dies are stacked on one another.

In hybrid bonding, conductive pads on a top surface of one die may be directly bonded to conductive pads on a top surface of the other die, for example, using fusion bonding and annealing processes. However, as a result of the annealing process, the material of the conductive pads may be stretched (e.g., as a result of increased ductility) and voids may be formed between the bonded conductive pads, especially in the corner regions.

## BRIEF DESCRIPTION OF THE DRAWINGS

For a more complete understanding of the present invention, and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

FIG. **1** illustrates a cross-sectional view of a device die in accordance with various embodiments;

FIG. **2** illustrates a cross-sectional view of patterning an opening in the device die in accordance with various embodiments;

FIG. **3** illustrates a cross-sectional view of forming a liner over the device die and in the opening in accordance with various embodiments;

FIG. **4** illustrates a cross-sectional view of extending the opening further into the device die in accordance with various embodiments;

FIG. **5** illustrates a cross-sectional view of removing the liner from the device die in accordance with various embodiments;

FIG. **6** illustrates a cross-sectional view of filling the opening in the device die with a conductive material in accordance with various embodiments;

FIG. **7** illustrates planarizing a surface of the device die in accordance with various embodiments;

FIG. **8**A illustrates bonding an oxide layer of the device die to another oxide layer of another device die in accordance with various embodiments;

FIG. **8**B illustrates a top-down view of a bonding tool, which may be used to bond the device dies in accordance with various embodiments;

FIG. **9** illustrates bonding conductive pads of the device dies in accordance with various embodiments;

FIG. **10** illustrates a flow chart of a process flow for forming conductive pads and hybrid bonding device dies in accordance with various embodiments; and

FIGS. **11**A through **11**C illustrate varying views of a bonded image sensing device in accordance with various embodiments.

Corresponding numerals and symbols in the different figures generally refer to corresponding parts unless otherwise indicated. The figures are drawn to clearly illustrate the relevant aspects of the embodiments and are not necessarily drawn to scale.

## DETAILED DESCRIPTION OF ILLUSTRATIVE EMBODIMENTS

The making and using of the embodiments of the disclosure are discussed in detail below. It should be appreciated, however, that the embodiments provide many applicable inventive concepts that can be embodied in a wide variety of specific contexts. The specific embodiments discussed are merely illustrative, and do not limit the scope of the disclosure.

A conductive pad structure for hybrid bonding and the method of forming the same are provided in accordance with an embodiment. The intermediate stages of manufacturing an embodiment are illustrated. The variations of the embodiments are then discussed.

Embodiments will be described with respect to a specific context, namely hybrid bonding of stacked device dies for image sensing. Other embodiments may also be applied, however, to other applications of bonding device dies such as in 3DIC packages.

FIGS. **1** through **9** illustrate cross-sectional views of intermediary steps of forming a conductive pad for hybrid bonding in accordance with various embodiments. FIG. **1** illustrates a cross-sectional view of a portion of a first device die **100**. In image sensing technologies, first device die **100** may include photodiodes interconnected to form a pixel array. First device die **100** includes a substrate **102**, which may be a bulk silicon substrate although other semiconductor materials including group III, group IV, and group V elements may also be used. Alternatively, substrate **102** may be a silicon-on-insulator (SOI) substrate. Active devices (not shown) such as transistors and photodiodes may be formed on the top surface of substrate **102**.

First device die **100** further includes interconnect layers **104** formed over substrate **102**. Interconnect layers **104** may include an inter-layer dielectric (ILD) and/or inter-metal dielectric layers (IMD) containing conductive features (e.g., metal lines and vias, not shown) formed over substrate **102** using any suitable method. Interconnect layers **104** may connect various active devices in substrate **102** to form functional circuits. The ILD/IMDs may comprise low-k dielectric materials having k values, for example, lower than about 4.0 or even 2.8. In some embodiments, interconnect layers **104** may comprise un-doped silicate glass (USG), and the like. Interconnect layers **104** may have a thickness of about 2200 Å although the actual dimensions of interconnect layers **104** may vary depending on layout design.

An isolation layer **106** may be formed over interconnect layers **104**. Isolation layer **106** may comprise silicon nitride, silicon oxide, or the like. Isolation layer **106** may have a thickness of about 500 Å, although the actual dimension isolation layer **106** may vary depending on layout design.

Redistribution layers (RDLs) **108** may be formed over isolation layer **106**. RDLs **108** may comprise polymer layers or dielectric layers (e.g., comprising USG) having interconnect structures (e.g., metal lines and vias) that route the electrical circuits formed in interconnect layers **104** to desired locations in first device die **100**. RDLs **108** may have a thickness of about 3000 Å, although the actual dimensions RDLs **108** may vary depending on layout design.

An oxide layer **110** is formed on a top surface of first device die **100**. Oxide layer **110** may comprise silicon oxynitride (SiON), $SiO_2$, SiN, SiC, or the like. Oxide layer **110** may have a thickness of about 3000 Å and may be used as a bonding interface layer for bonding first device die **100** to another device die during a subsequent hybrid bonding process (described further herein in FIGS. **8** and **9**). Although oxide layer **110** is described herein as an oxide layer, any interfacial layer suitable for direct bonding to another interfacial layer (e.g., through fusion bonding) may be used in alternative embodiments in lieu of an oxide.

FIG. **2** illustrates the patterning of first device die **100** to form an opening **112** for a conductive pad. First device die **100** may be patterned, for example, using a combination of photolithography and etching. While FIG. **2** illustrates opening **112** extending through oxide layer **110** into RDLs **108**, the layers of first device die **100** that are patterned for opening **112** may vary depending on a desired depth of opening **112**. For example, opening **112** may have a depth from a top surface of first device die **100** of between about 0.1 μm and about 1 μm.

FIG. **3** illustrates the formation of a liner **114** over oxide layer **110** and covering sidewalls and a bottom surface of opening **112**. Liner **114** may be deposited using any conformal deposition method such as chemical vapor deposition (CVD), or the like. Liner **114** may comprise silicon nitride, titanium nitride, titanium oxide, or any material that may be removed at a greater rate than oxide layer **110** and RDLs **108**. In various embodiments, liner **114** may be between about 300 Å and about 1000 Å or more thick.

FIG. **4** illustrates another patterning of first device die **100** to extend opening **112** further into first device die **100**. This second patterning may be achieved, for example, using an anisotropic etching process so that the vertical dimension of opening **112** is increased without substantially increasing the horizontal dimensions of opening **112**. As a result of the patterning, lateral portions of liner **114** (e.g., covering oxide layer **110** and bottom surfaces of opening **112**) may be removed. That is, a top surface of oxide layer **110** may be exposed. Vertical portions of liner **114** (e.g., on sidewalls of opening **112**) may remain in first device die **100**. After the second patterning, liner **114** may only partially cover sidewalls of opening **112**. Furthermore, as a result of the patterning, oxide layer **110** may be thinned. For example, in embodiments where oxide layer **110** was deposited to have a thickness of about 5000 Å, after the patterning, oxide layer **110** may have a thickness of about 2500 Å. Furthermore, because the etching rate of liner **114** may be greater than the etching rate of oxide layer **110**, less oxide layer **110** may be removed than liner **114** during etching. Thus, a top surface of oxide layer **110** may or may not be substantially level with a top surface of liner **114**.

While FIG. **4** illustrates opening **112** extending through oxide layer **110**, RDLs **108**, and isolation layer **106** into interconnect layers **104**, the layers of first device die **100** that are patterned to extend opening **112** may vary depending on a desired depth of opening **112**. For example, opening **112** may have a depth from a top surface of first device die **100** after expansion of between about 0.2 μm and about 2 μm.

In FIG. **5**, remaining portions of liner **114** are selectively removed using any suitable method, such as an etching process using a chemical etchant that etches liner **114** at a faster rate than device layers contacting liner **114** (e.g., oxide layer **110** and RDLs **108**). For example, a solution of 85% phosphoric acid ($H_3PO_4$) may be used when liner **114** comprises SiN, oxide layer **110** comprises SiON, and RDLs **108** comprise USG. The exact chemistry used during etching may vary depending on the materials used to form the applicable device layers in first device die **100**. In various embodiments, a ratio of removal rates of liner **114** to oxide layer **110** to RDLs **108** may be about 60 to 30 to 1. Furthermore, because oxide layer **110** may have a higher removal rate than RDLs **108**, sidewalls of oxide layer **110** may or may not be vertically aligned with sidewalls of RDLs **108** in opening **112**.

As a result of removing liner **114**, a top portion of opening **112** has a horizontal dimension W1 that is larger than a horizontal dimension W2 of a bottom portion of opening **112**. Horizontal dimensions W1 and W2 may be a length/width, diameter, or the like depending on a top down shape of opening **112**. In various embodiments, horizontal dimensions W1 and W2 may be between about 0.1 μm and 10 μm. A difference in dimension between W1 and W2 may depend on the thickness of liner **114**. For example, in embodiments where liner **114** was about 500 Å thick, W1 may be about 0.1 μm larger than W2. Generally, a difference between W1 and W2 may be at least about 0.05 μm.

FIG. **6** illustrates the filling of opening **112** with a conductive material **116**, for example, copper or a copper alloy. The filling of opening **112** may include an electro-chemical plating (ECP) process. Conductive material **116** may overflow opening **112** and cover a top surface of oxide layer **110**. In various embodiments, a barrier layer (not shown) and/or a seed layer (not shown) may be formed, for example, using physical vapor deposition, CVD, or the like in opening **112** prior to the filling of opening **112** with conductive material **116**.

Subsequently, as illustrated by FIG. **7**, a planarization (e.g., a chemical mechanical polish (CMP)) may be performed to remove overflow portions of conductive material **116** to form conductive pad **118** in first device die **100**. The planarization may result in the dishing of conductive pad **118** (i.e., a top surface of conductive pad **118** may be non-planar and concave). This dishing may be intentional to allow room for conductive pad **118** to expand in a subsequent annealing process. The dishing may remove a depth H1 of conductive pad **118**, and the planarization process may be controlled so that depth H1 is less than about 50 Å to ensure proper bonding of first device die **100** to another device die.

As a result of the process steps illustrated by FIGS. **1** through **7**, conductive pad **118** is formed in first device die **100**. Additionally, in an embodiment, conductive pad **118** is formed of a single continuous material (e.g., copper) having no internal interfaces formed therein. Conductive pad **118** is shaped to include a top portion having a horizontal dimension W1 and a vertical dimension H2. Conductive pad **118** further includes a bottom portion having a horizontal dimension W2 and a vertical dimension H3. In various embodiments, horizontal dimension W1 is larger than horizontal dimension W2. Horizontal dimensions W1 and W2 may be between about 0.1 μm and about 10 μm. Horizontal dimensions W1 and W2 may be a length/width, diameter, or the like depending on a top-down shape of conductive pad **118**. Centerlines of the top and bottom portions may be vertically aligned.

In a top down view, conductive pad **118** may have any shape such as a square, rectangle, circle, oval, or the like. Furthermore, vertical dimensions H**1** and H**2** of the top and bottom portions of conductive pad **118**, respectively, may or may not be equal, and vertical dimensions H**1** and H**2** may be between about 0.1 μm and about 1 μm.

Thus, as illustrated by FIG. **7**, the shape of conductive pad **118** provides for additional metallic material in center regions **118**A of conductive pad **118** compared to corner regions **118**B of conductive pad **118**. This shape of conductive pad **118** reduces the overall surface stress of conductive pad **118**. For example, in simulations where conductive pad **118** comprises copper and the dimensions of W**1**, W**2**, H**2**, and H**3** are 1 μm, 0.5 μm, 0.5 μm, and 1 μm, respectively, the thermal stress at the surface of conductive pad **118** is $4.938\times10^{-5}$ Newtons. However, in simulations where the dimensions of W**1**, W**2**, H**2**, and H**3** were 1 μm, 0 μm, 0.5 μm, and 0 μm, respectively, (e.g., where the metallic material was uniformly distributed), the surface stress of the conductive pad was higher at $5.977\times10^{-5}$ Newtons. The reduction of surface stress reduces the probability of forming voids, particularly in corner regions **118**B, during subsequent bonding processes. Although FIG. **7** only illustrates first device die **100** having a single conductive pad **118**, first device die **100** may include multiple conductive pads **118** formed simultaneously.

FIGS. **8**A through **9** illustrate the bonding of first device die **100** to a second device die **200** through hybrid bonding. In image sensing technologies, second device die **200** may include logical control circuits for controlling the pixel array in first device die **100**. Second device die **200** may include a substrate **202** (e.g., having active devices, not shown), interconnect layers **204** (e.g., forming logic control circuits), an isolation layer **206**, RDLs **208**, and an oxide layer **210**. The various layers of second device die **200** may be substantially similar to the layers of first device die **100**, and detailed description of these device layers is omitted for brevity. Second device die **200** further includes a conductive pad **218**, which may be substantially similar in shape to conductive pad **118**.

FIG. **8**A illustrates the bonding of oxide layers **110** and **210** using, for example, a fusion bonding process. In various embodiments, the fusion bonding may be done using a bonding tool **300** illustrated in FIG. **8**B. The bonding may begin by loading first device die **100** and second device die **200** into load ports **302**A and **302**B, respectively. A movement module **304** may move first device die **100** to a surface activation module **306**. In an embodiment, surface activation module **306** may be a plasma module that exposes the surface of oxide layer **110** to a plasma environment. Alternatively, surface activation module **306** may be a wet cleaning module that performs a wet clean to activate the surface of oxide layer **110**. For example, oxide layer **110** may be cleaned using a procedure such as an SC-1 or SC-2 cleaning procedure to form a hydrophilic surface. In yet another alternative, surface activation module **306** may be an etching module that treats the surface of oxide layer **110** to form a hydrophobic surface, for example, using an etching solution of hydrogen fluoride (HF) or ammonium fluoride ($NH_4F$).

Subsequently, movement module **304** may move first device die **100** to a cleaning module **308** to clean the surface of oxide layer **110**. Movement module **304** may move first device die **100** to a bonding module **310** to await bonding. Movement module **304** may also move second device die **200** to surface activation module **306**. A similar surface activation treatment may be applied to a surface of oxide layer **210** as the treatment applied to oxide layer **110**. For example, a plasma treatment, wet cleaning, or etching may be applied to the surface of oxide layer **210** depending on the surface activation process used on oxide layer **110**. Subsequently, the movement module **304** may move second device die **200** to cleaning module **308** to clean the surface of oxide layer **210**, and second device die **200** may be moved to bonding module **310** for bonding with first device die **100**.

Bonding module **310** may include an alignment tool to align oxide layers **110** and **210** of first device die **100** and second device die **200**. Oxide layers **110** and **210** are then contacted together to begin the hybrid bonding procedure. At this stage, conductive pads **118** and **218** may not be bonded, and a void **120** may be disposed between conductive pads **118** and **218** due to dishing.

After oxide layer **110** is in contact with oxide layer **210**, a thermal annealing process may be utilized to strengthen the bond between oxide layers **110** and **210** and to additionally bond conductive pads **118** and **218** as illustrated by FIG. **9**. The annealing process conditions may include increasing the temperature of first and second device dies **100** and **200** from room temperature (e.g., about 20° Celsius (C.)) to a suitable annealing temperature (e.g., between about 150° C. and about 400° C.) at a rate of 5° C. per minute. The temperature of first and second device dies **100** and **200** may be maintained at the annealing temperature for about two hours. The annealing process expands the conductive material of conductive pads **118** and **218** to fill void **120**, bonding conductive pads **118** and **218** and electrically connecting first and second device dies **100** and **200**. As a result of the shape of conductive pads **118** and **218** and reduced surface stress, the bonded conductive pads **118** and **218** may be substantially free of voids. Furthermore, the reduced surface stress may allow for the annealing process to be performed in easier process conditions (e.g., at a lower temperature).

FIG. **10** illustrates a process flow **400** for hybrid bonding device dies in accordance with various embodiments. In step **402**, a die (e.g., first device die **100**) is patterned to form an opening. The die may include an oxide layer (e.g., oxide layer **110**) at a top surface, which may be used as a bonding interface in hybrid bonding. Next, in step **404**, a liner (e.g., liner **114**) is formed over the die and covering sidewalls and a bottom surface of the opening. The liner may be formed of any material that may be selectively removed at a greater rate than any layers of first device die **100** in physical contact with the liner.

In step **406**, another etching is performed in first device die **100** to expand the opening further into the die, for example, using an anisotropic etching process. The anisotropic etching may not substantially expand the opening in a lateral direction. As a result of the etching, lateral portions of the liner (e.g., covering a top surface of the die and bottom surface of the opening) may be removed. Remaining portions of the liner on sidewalls of the opening may not be removed and may partially cover sidewalls of the expanded opening.

In step **408**, the liner is removed, for example by selecting a chemical etchant that selectively removes the liner without significantly removing other portions of the device die. For example, when the liner comprises SiN and the other device layers in contact with the liner comprise SiON and USG, a solution of 85% phosphoric acid may be used to remove the liner. As a result of removing the liner, a top portion of the opening may have a first width that is larger than a second width of a bottom portion of the opening.

In step **410**, the opening is filled with a metallic material (e.g., copper). The filling of the metallic material may overflow the opening. Subsequently, in step **412**, a CMP may be performed to remove excess metallic material to form a conductive pad. The CMP process may further dish a top surface of the conductive pad (i.e., form a non-planar, concave top surface). This dishing may be intentional to allow expansion room for the conductive pad during a subsequent bonding process. The resulting conductive pad may have a center portions having additional conductive material than corner portions. This shape of the resulting conductive pad reduces the thermal stress on a top surface of the conductive pad.

In step **414**, the oxide layer of the die may be bonded (e.g., fusion bonded) to an oxide layer of another device die. The other device die may also have a second conductive pad that is substantially similar, particularly in shape, to the conductive pad formed in steps **402** through **412**. The bonding of the oxide layers may not bond the conductive pads, and a void may be defined between the conductive pads due to dishing.

Finally, in step **416**, an annealing process is performed to bond the two conductive pads and fill the void. The annealing process may be performed by ramping up the temperature of the bonded dies from room temperature to 300° C. at a rate of 5° C. per minute. The temperature of the bonded dies may be maintained at about 300° C. for about two hours. As a result of the shape of the conductive pads and the reduced thermal stress, the resulting bonded conductive pads may be substantially free of any voids.

FIGS. **11**A through **11**C illustrate varying views of a bonded first and second device dies **100** and **200** in an example embodiment where first device die **100** is a CMOS image sensor (CIS) die and second device die **200** is a logic control die. FIG. **11**A shows a cross-sectional view, FIG. **11**B illustrates an in-depth view of the cross-sectional view of FIG. **11**A, and FIG. **11**C illustrates a top down view. First device die **100** may include photodiodes **101**, transfer transistors **103**, and metallization layers **105** (e.g., interconnect layers **104**). Metallization layers **105** may electrically connect photodiodes **101** and transfer transistors **103** to form functional circuits. These functional circuits may include a pixel array in a center region of first device die **100** as illustrated by FIG. **11**C. The functional circuits of first device die **100** may also include an analogue to digital convertor (ADC) **107**, correlated double sampling (CDS) circuits **109**, a row decoder **111**, and the like. As also illustrated by FIG. **11**C, a plurality of conductive pads **118** for bonding may be disposed on peripheral regions of first device die **100**.

Second device die **200** may include logic arrays **201** and metallization layers **205** (e.g., interconnect layers **204**). The metallization layers may interconnect logic arrays **201** to form digital signal processing circuits (e.g., application specific integrated circuits (ASIC)) that provide control functions for the image sensor formed by first device die **100** and second device dies **200** as also illustrated by FIG. **11**C. A plurality of conductive pads **218** may be located at peripheral regions the top surface of second device die **200**.

FIG. **11**B illustrates a detailed cross-sectional view of a portion **100**A/**200**A of bonded first and second device dies **100** and **200**. Hybrid bonding may be used to bond oxide layer **110** and conductive pads **118** of first device die **100** to oxide layer **210** and conductive pads **218** of second device die **200**, respectively. Conductive pads **118** and **218** are shaped so that center portions of conductive pads **118** and **218** are thicker (e.g., has more conductive material) than corner regions of conductive pads **118** and **218**. This shape of conductive pads **118** and **218** reduces thermal stress at the interface between conductive pads **118** and **218**, which reduces the formation of voids after hybrid bonding.

In accordance with an embodiment, a method includes patterning an opening through a layer at a surface of a device die. The method further includes forming a liner on sidewalls of the opening, patterning the device die to extend the opening further into the device die. After patterning the device die, the liner is removed. A conductive pad is formed in the device die by filling the opening with a conductive material.

In accordance with another embodiment, a method includes etching a first opening through an oxide layer on a surface of a first device die. The first opening has a first horizontal dimension. A liner is formed over the first device die. The liner covers sidewalls and a bottom surface of the first opening. The method further includes etching a second opening connected to the first opening in the first device die by etching through first portions of the liner on the bottom surface of the first opening. The second opening has a second horizontal dimension smaller than the first horizontal dimension. Second portions of the liner on sidewalls of the first opening are removed. A first conductive pad is formed in the first and second openings, and the first device die is bonded to a second device die. The first conductive pad is bonded to a second conductive pad on a surface of the second device die.

In accordance with yet another embodiment, a device includes an oxide layer at a top surface of a device die and a conductive pad in the device die. The conductive pad includes a top portion at the top surface of the first device die having a first horizontal dimension and a bottom portion connected to the top portion with no internal interface between the top portion and the bottom portion. The bottom portion has a second horizontal dimension, and the first horizontal dimension is larger than the second horizontal dimension.

While this invention has been described with reference to illustrative embodiments, this description is not intended to be construed in a limiting sense. Various modifications and combinations of the illustrative embodiments, as well as other embodiments of the invention, will be apparent to persons skilled in the art upon reference to the description. It is therefore intended that the appended claims encompass any such modifications or embodiments.

What is claimed is:

**1**. A method comprising:

patterning an opening through a first layer at a surface of a first device die;

forming a liner on a top surface of the first layer and sidewalls of the opening;

patterning the first device die to extend the opening further into the first device die, wherein patterning the first device die to extend the opening comprises removing portions of the liner using an etching process that etches the liner at a faster rate than the first layer;

removing the liner after the patterning the first device die; and

forming a first conductive pad in the first device die by filling the opening with a conductive material.

**2**. The method of claim **1**, further comprising bonding the first device die to a second device die using a hybrid bonding process, wherein the hybrid bonding process comprises:

fusion bonding the first layer to a second oxide layer disposed on a surface of the second device die; and

bonding the first conductive pad to a second conductive pad in the second device die, wherein the bonding the first conductive pad to the second conductive pad is performed at least in part using an annealing process.

3. The method of claim 2, wherein the annealing process comprises increasing a temperature of the first device die and the second device die from room temperature to about 300° Celsius at a rate of about 5° Celsius per minute, and maintaining the temperature of the first device die and the second device die at about 300° Celsius for about two hours.

4. The method of claim 2, wherein the second conductive pad has substantially a same shape as the first conductive pad.

5. The method of claim 2, wherein the annealing process fills a void disposed between the first conductive pad and the second conductive pad when the first device die is contacted to the second device die.

6. The method of claim 1, wherein the patterning the first device die to extend the opening comprises an anisotropic etching process.

7. The method of claim 1, wherein the removing the liner comprises an etching process using a chemical etchant that selectively removes the liner at a first removal rate and the first layer at a second removal rate, and wherein the first removal rate is greater than the second removal rate.

8. The method of claim 7, wherein the chemical etchant removes device layers contacting the liner at a third removal rate, and wherein a ratio of the first removal rate to the second removal rate to the third removal rate is sixty to thirty to one.

9. The method of claim 7, wherein the liner comprises silicon nitride and the first layer comprises silicon oxynitride, and wherein the chemical etchant comprises a solution of 85 percent phosphoric acid.

10. The method of claim 1, wherein the forming the first conductive pad comprises:

overfilling the opening with a metallic material, wherein the metallic material covers the first layer; and

polishing excess portions of the metallic material to expose the first layer, wherein the polishing causes a top surface of the first conductive pad to be concave.

11. A method comprising:

etching a first opening through a first oxide layer on a surface of a first device die, wherein the first opening has a first horizontal dimension, and wherein the first opening further extends into a dielectric layer under the first oxide layer;

forming a liner contacting a top surface of the first oxide layer, wherein the liner covers sidewalls and a bottom surface of the first opening;

etching a second opening connected to the first opening in the first device die by etching through first portions of the liner on the bottom surface of the first opening, wherein the second opening has a second horizontal dimension smaller than the first horizontal dimension, and wherein etching the second opening comprises using a chemical etchant that etches the first oxide layer at a slower rate than the liner;

removing second portions of the liner on sidewalls of the first opening; and

forming a first conductive pad in the first opening and the second opening.

12. The method of claim 11, further comprising bonding the first device die to a second device die, wherein the first conductive pad is bonded to a second conductive pad on a surface of the second device die, wherein the first conductive pad and the second conductive pad have substantially a same shape.

13. The method of claim 12, wherein the bonding the first device die comprises:

fusion bonding the first oxide layer to a second oxide layer on the surface of the second device die; and

annealing the first device die and the second device die to electrically connect the first conductive pad to the second conductive pad.

14. The method of claim 11, wherein the forming the first conductive pad comprises:

overfilling the first opening and the second opening with a metallic material; and

exposing the first oxide layer by removing excess portions of the metallic material using a chemical-mechanical polish (CMP) process, wherein the CMP process causes dishing on a top surface of the first conductive pad.

15. The method of claim 14, wherein the dishing on the top surface of the first conductive pad is controlled so that a height difference between the top surface of the first conductive pad and a top surface of the first oxide layer is less than about 50 Å.

16. A method comprising:

patterning a first opening extending through a first dielectric layer at a top surface of a first die, wherein the first opening comprises:

a first portion in the first dielectric layer; and

a second portion under the first portion, wherein the first portion is wider than the second portion;

filling the first opening with a conductive material to form a first conductive pad;

providing a second die comprising a second conductive pad extending through a second dielectric layer at a top surface of the second die;

aligning the first conductive pad to the second conductive pad;

bonding the first dielectric layer to the second dielectric layer, wherein after bonding the first dielectric layer to the second dielectric layer, a void is disposed between the first conductive pad and the second conductive pad; and

annealing the first die and the second die to bond the first conductive pad to the second conductive pad, wherein annealing the first die and the second die fills the void.

17. The method of claim 16, wherein patterning the first opening comprises:

patterning the first portion of the first opening in the first die;

forming a liner on sidewalls of the first portion of the first opening;

after forming the liner, anisotropically etching the first die to form the second portion of the first opening; and

removing remaining portions of the liner using an etching process that etches the liner at a faster rate than the first dielectric layer.

18. The method of claim 17, wherein the liner is disposed on lateral surfaces of the first die, and wherein anisotropically etching the first die comprises removing portions of the liner on the lateral surfaces of the first die.

19. The method of claim 16 wherein the second conductive pad comprises first width in the second dielectric layer and a second width under the second dielectric layer, wherein the first width is greater than the second width.

20. The method of claim 16, wherein the first conductive pad is disposed at a peripheral region of the first die, and wherein the second conductive pad is disposed at a peripheral region of the second die.

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